(FILE 'USPAT' ENTERED AT 13:51:13 ON 18 APR 1997)

SET PAGE SCROLL
L1 105 S 395/281/CCLS
L2 0 S STRAATS, ERIK/IN
L3 72 S (ISOCHRONOUS OR ISOCHRONAL) (P) CHANNELS
L4 2 S L3 AND NODES AND TRANSCEIVER
L5 1 S L4 AND (BUFFERS OR MEMORY) AND INTERRUPT

=> d l4 1-2

1. 5,566,169, Oct. 15, 1996, Data communication network with transfer port, cascade port and/or frame synchronizing signal; Geetha N. K. Rangan, et al., 370/366, 352, 426 [IMAGE AVAILABLE]

2. 5,440,556, Aug. 8, 1995, Low power isochronous networking mode; Brian C. Edem, et al., 370/465; 340/825.02; 370/509; 375/214, 219, 257, 354; 455/38.3, 343 [IMAGE AVAILABLE]

=> d l5

1. 5,566,169, Oct. 15, 1996, Data communication network with transfer port, cascade port and/or frame synchronizing signal; Geetha N. K. Rangan, et al., 370/366, 352, 426 [IMAGE AVAILABLE]

=>

5,617,418

5,406,559

(FILE 'USPAT' ENTERED AT 15:31:23 ON 18 APR 1997)

SET PAGE SCROLL
L1 0 S 5406559/PN AND INTERRUP
L2 0 S 5617418/PN AND INTERRUPT
L3 0 S 5440556/PN AND INTERRUPT
L4 1 S 5566169/PN AND INTERRUPT

=> d

1. 5,566,169, Oct. 15, 1996, Data communication network with transfer port, cascade port and/or frame synchronizing signal; Geetha N. K. Rangan, et al., 370/366, 352, 426 [IMAGE AVAILABLE]

=> d kwic
US PAT NO: 5,566,169 [IMAGE AVAILABLE] L4: 1 of 1

DETDESC:

DETD(42)

Status . . . each of the six status bits indicating port activity, low power mode, port isochronous capacity, P or physical layer portion **interrupt** and D **interrupt**, there is a corresponding register. The 6th status bit, indicating cascade mode for port 1, is used to control the. . . the appropriate logic to allow cascading of i hubs. Whenever a port's activity or capacity or power mode changes, an **interrupt** is generated. For P or physical layer and D channels,interrupts are generated as long as the corresponding physical layer is waiting to be serviced and physical layer and D channel **interrupt** status bits are active.

DETDESC:

DETD(43)

An . . . giving a physical layer device address. For example, if any physical layer device's activity changes, it results in a single **interrupt**. The processor may read the corresponding register to determine all the active and inactive physical layer devices. In the absence. . .

DETDESC:

DETD(60)

If . . . for the RX.sub.-- ram buffer. If a port's data has "bad parity," data is loaded into the buffer. However, an **interrupt**, indicating that "bad parity is received" is generated. If data has "bad parity" there is an option to either regenerate. . .

DETDESC:

DETD(67)

The . . . hub in the status data of that port. Preferably, a change in the state of this bit will cause an **interrupt** to the processor unless masked.

DETDESC:

DETD(69)

The . . . such as the 15.872 Mbps isochronous bandwidth capacity. Preferably, a change in the state of this bit will cause an **interrupt** to the processor unless masked.

DETDESC:

DETD(70)

The . . . channel receiver or transmitter needs to be processed by the host processor. Preferably, this bit being set will generate an **interrupt** to the processor unless masked. When the processor processes an **interrupt** from the physical layer or isochronous switching device, it first reads the **Interrupt** Status Register (ISR) to determine the source of the **interrupt**. Upon reading this **interrupt** and a D channel **Interrupt** indicated, the processor upon reading the Port D Channel **Interrupt** Register, will know which ports are requesting D channel servicing.

DETDESC:

DETD(71)

The . . . a physical layer device needs to be processed by the host processor. Preferably, this bit being set will generate an **interrupt** to the processor unless masked. When the processor processes an **interrupt** from the isochronous switching device, it first reads the **Interrupt** Status Register (ISR) to determine the source of the **interrupt**. Upon reading this **interrupt** and a Physical layer **Interrupt** indicated, the processor upon reading the Port Physical layer **Interrupt** Register, will know which ports are requesting Physical layer servicing.

DETDESC:

DETD(77)

In . . . isochronous switching device is used to notify the host processor which of the node's D channel requires processing. Thus, the **interrupt** is centralized. This makes the D channel processing more efficient since a processor does not have to continuously poll all. . .

DETDESC:

DETD(78)

The . . . passes between the hub and node physical layers. The isochronous switching device is used to centralize the attached node's maintenance **interrupt** via the PINT requests. This makes the M channel processing more efficient since a processor does not have to be. . .

NAMA SYSTEM
4/18/97

E003 WORD FREQUENCY SEARCH REPORT

Classification Analysis:

1. 364/DIG. 1 Total=18 ORs=0 XRs=18
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub DIG. 1 GENERAL PURPOSE PROGRAMMABLE DIGITAL COMPUTER SYSTEMS

2. 364/239 Total=9 ORs=0 XRs=9
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub ???.6 INTERFACING OR COMMUNICATION TECHNIQUE
   Sub 239 .Buffer/interface function

3. 395/250 Total=9 ORs=3 XRs=6
   Class 395 INFORMATION PROCESSING SYSTEM ORGANIZATION
   Sub 200.01 MULTICOMPUTER DATA TRANSFERRING
   Sub 250 .Buffering for speed changing

4. 364/240 Total=7 ORs=0 XRs=7
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub ???.6 INTERFACING OR COMMUNICATION TECHNIQUE
   Sub 240 .Bus

5. 364/DIG. 2 Total=7 ORs=0 XRs=7
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub DIG. 2 GENERAL PURPOSE PROGRAMMABLE DIGITAL COMPUTER SYSTEMS

6. 364/239.1 Total=5 ORs=0 XRs=5
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub ???.6 INTERFACING OR COMMUNICATION TECHNIQUE
   Sub 239 .Buffer/interface function
   Sub 239.1 ..Rate control

7. 364/242.3 Total=5 ORs=0 XRs=5
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub ???.6 INTERFACING OR COMMUNICATION TECHNIQUE
   Sub 242.3 .Direct access/DMA

8. 364/242.94 Total=5 ORs=0 XRs=5
   Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
   Sub ???.6 INTERFACING OR COMMUNICATION TECHNIQUE
   Sub 242.94 .Networking

9. 364/284 Total=5 ORs=0 XRs=5
Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
Sub ???.15 SYSTEM MANAGEMENT (SOFTWARE)
Sub 284 .Communication

10. 395/308 Total=5 ORs=0 XRs=5
Class 395 INFORMATION PROCESSING SYSTEM ORGANIZATION
Sub 280 INTRASYSTEM CONNECTION
Sub 306 .Bus architecture
Sub 308 ..Dual bus systems

11. 395/800 Total=5 ORs=1 XRs=4
Class 395 INFORMATION PROCESSING SYSTEM ORGANIZATION
Sub 800 PROCESSING ARCHITECTURE

US PAT NO: **5,406,559** [IMAGE AVAILABLE] L3: 1 of 1

ABSTRACT:
A data transfer **delay** compensation system for a data communications system having a first transceiver and a second transceiver wherein the first transceiver includes circuitry for transferring an external cycle reference signal and a cycle **delay** signal to the second transceiver. The second transceiver includes circuitry for transmitting the received cycle reference back to the first. . . a phase difference between the received cycle reference and the external cycle reference signal in order to update the cycle **delay** signal.

SUMMARY:

BSUM(13)

According to one embodiment of the present invention, the hub-node system includes **delay** circuitry to compensate for cycle misalignments caused by system cabling. The **delay** system operates to minimize the amount of data buffering required. In the **delay** system of the present invention, the hub times the **delay** between the transmission of the cycle start and the arrival of the received cycle start. The hub thus senses the adjustment necessary in the node's cycle and outputs a control signal to the node. At the node, a **delay** circuit stores the **delay** value and delays the start of the cycle reference provided to the node transmitter. The node transmitter thus outputs cycles. . .

SUMMARY:

BSUM(14)

According to another embodiment of the invention, the node **delay** circuitry comprises a latch controlled by the hub. The latch triggers when the cycle reference is provided to the node. . .

DRAWING DESC:

DRWD(16)

FIG. 11 is a block diagram of node circuitry having a **delay** circuit according to an embodiment of the present invention;

DETDESC:

DETD(34)

FIG. 10 depicts a timing scheme to reduce **delay** and jitter to enable the buffering operation described in the paragraphs above. As shown in FIG. 10, the timing can. . . the hub lags the time when the frame was sent from the hub as shown by time line 218. A **delay** 220 is therefore introduced before the node begins transmission of the next frame to hub 222. **Delay** 220 accounts for the latency introduced by transmission over physical media 46 and encoding delays introduced by the hub and. . .

DETDESC:

DETD(35)

The hub makes a measurement of the amount of adjustment to be made to the nodes cycle **delay**. This can be done by timing the **delay** between the transmission of the cycle start and the arrival of the received cycle start. This adjustment can then be. . . The arrival value would be added to the current value, with the modified value to be used as the cycle **delay**.

DETDESC:

DETD(36)

Another scheme for adjusting **delay** transmits a signal to the node which indicates that the cycle **delay** is to be increased. Every cycle that this increase parameter is received, the node increases the cycle **delay**. The advantage is in the use of a counter to hold the cycle **delay** value but requires multiple cycles to correct the skew.

DETDESC:

DETD(37)

FIG. 11 is a block diagram of **delay** circuitry useful for aligning the transmitted and received data to compensate for line delays. The **delay** circuitry of FIG. 11 comprises a data control circuit 226. Control circuit 226 may comprise a finite state machine and adder and/or register circuitry. Circuit 226 may store a known, fixed initial value of **delay** for each of the nodes coupled to the hub 44. Latch 236 could also be initialized to a known fixed **delay**. For cable lengths under 100M, this and the small FIFO proves suitable. An adjustable **delay** accommodates longer lengths, such as with fiber optics. The adjustable **delay** value is output as a stream of control bits, together with the cycle reference frame, by hub transmitter 228 over. . .

DETDESC:

DETD(38)

At node receiver 230, the cycle reference is extracted and provided to node **delay** circuit 232. The **delay** control bits are provided to node data control circuit 234. Node data control circuit 234 may also comprise a state. . .

DETDESC:

DETD(39)

The . . . According to one embodiment of the present invention circuit 236 is a memory or counter device that stores the current **delay** value and outputs this value to **delay** circuit 232. **Delay** circuit 232 then waits a period of time, t, as given by the output of circuit 236 before transmitting the. . .

DETDESC:

DETD(40)

Data . . . hub receiver 240 over physical media 46. Hub receiver 240

extracts the transmitted cycle reference and outputs this data to **delay** measurement circuit 244. **Delay** measurement circuit 244 compares the cycle reference received from the node to the external cycle reference to obtain an offset. . . .

DETDESC:

DETD(41)

Offset value 246 is provided to hub data control circuit 226. Offset value 246 indicates the **delay** required to align the received and transmitted data. When the offset value is zero, the received and transmitted frames are in phase. The offset value may be used to increment the initial **delay** value stored in circuit 226, or be added to the current **delay** value stored in circuit 226 to obtain a new current **delay** value for output to the node.

DETDESC:

DETD(42)

The **delay** circuitry of the present invention accommodates all lengths of cable up to a cycle reference length of **delay**. Other delays can also be accommodated so long as the sum of delays is an integral number of frame cycles. Because the data is multiplexed, the **delay** circuit of the present invention also has the advantage of accommodating the delays of the many individual isochronous sources coupled. . . .

CLAIMS:

CLMS(1)

What . . . claimed is:

1. In an isochronous data communications system having a first transceiver and a second transceiver, a data transfer **delay** compensation system comprising:
means for transferring a cycle reference and a cycle **delay** signal from said first transceiver to said second transceiver wherein said means for transferring a cycle reference is coupled to. . . said cycle reference at said second transceiver, wherein said given time period varies according to a value of said cycle **delay** signal; and
means, coupled to said first transceiver, for measuring a phase difference between said cycle reference received at said first transceiver and said external cycle reference to update said value of said cycle **delay** signal.

CLAIMS:

CLMS(2)

2. . . .
first and second of said sources and sinks;
a transmitter in a hub for transmitting a cycle reference and a cycle **delay** signal at least to said first node;
at least a first and a second data link, said first link coupling said. . . coupling said second node with said hub;

a receiver in said first node for receiving said cycle reference and said cycle **delay** signal;
a transmitter in said first node for transmitting data to a receiver in said hub and said cycle reference at a given time period after receipt of said cycle reference according to a value of said cycle **delay** signal;
a multiplexer in said first node coupled to said transmitter in said first node, for transmitting data from both of. . . said cycle reference received at said hub receiver and an external cycle reference to update said value of said cycle **delay** signal.

CLAIMS:

CLMS(3)

3. . . . a communications system having a plurality of hubs coupled to exchange data between a plurality of nodes, a data transfer **delay** compensation system comprising:
a hub transmitter in one of said plurality of hubs, coupled to receive an external cycle reference, for transmitting a cycle reference, a cycle **delay** signal and isochronous data to at least one of said nodes;
a node receiver, coupled to said hub transmitter, for receiving said cycle reference, said cycle **delay** signal, and said isochronous data;
a node control circuit, coupled to said node receiver for receiving said cycle **delay** signal from said node receiver;
a node **delay** circuit, having an input coupled to receive said cycle reference from said node receiver and an output for delaying said. . . cycle reference;
an offset circuit having an input coupled to said node control circuit and an output coupled to said node **delay** circuit for controlling a **delay** time between receipt of said cycle reference at said input of said **delay** circuit and Said output of said cycle reference from said **delay** circuit;
a node transmitter, coupled to receive said cycle reference from said output of said node **delay** circuit, for transmitting said cycle reference to a hub receiver of said one hub;
a **delay** measurement circuit, coupled to said hub receiver, for receiving said cycle reference from said hub receiver, and coupled to said. . . and for outputting an offset value; and
a hub control circuit, coupled to receive said offset value for outputting said cycle **delay** signal to said hub transmitter.

CLAIMS:

CLMS(8)

8. . . . data transmissions between a first and a second data transceivers comprising the steps of:
transmitting a cycle reference and cycle **delay** signals from said first transceiver to said second transceiver;
forwarding said cycle reference from a receiver of said second transceiver to a **delay** circuit of said second transceiver;
delaying transfer of said cycle reference from said **delay** circuit to a transmitter of said second transceiver by a given amount of time period according to a value of said cycle **delay** signal;
transmitting said cycle reference from said second transceiver to said

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=> s 5406559/pn and (CPU or processor)
             1 5406559/PN
         47398 CPU
         94425 PROCESSOR
L4           1 5406559/PN AND (CPU OR PROCESSOR)
=> d kwic
US PAT NO:      **5,406,559** [IMAGE AVAILABLE]          L4: 1 of 1

DETDESC:

DETD(10)

 Hub . . . In an embodiment in which non-isochronous-sourced data
includes ethernet data, the hub circuitry 60 can be a standard ethernet
repeater **processor**. In this way, the system can be at least partially
backwards-compatible with previous ethernet hub systems.

DETDESC:

DETD(11)

 The D channel and maintenance data is provided to a signaling
**processor** 62. Signaling **processor** 62 performs various maintenance
and control functions such as identifying and alerting users of error
conditions, and setting up requested. . .

DETDESC:

DETD(25)

 The . . . the depicted embodiment, has been pre-established using the
D channel information. The D channel information is sent to a signaling
**processor** 138. The D channel information, which includes source,
destination, and other needed information, is used to store values in
preferably. . .

DETDESC:

DETD(29)

 Retrieval . . . ring is achieved by a multiplexer 156 controlled by a
control signal 158 output over line 160 from the signal **processor**
138, relying on a Table 162 in a fashion similar to that described for
control of multiplexer 146.
=> d his
     (FILE 'USPAT' ENTERED AT 15:02:07 ON 22 APR 1997)
L1           0 S 5440556/PN AND INTERRUPT
L2           0 S 5406559/PN AND INTERRUPT
L3           1 S 5406559/PN AND DELAY
L4           1 S 5406559/PN AND (CPU OR PROCESSOR)
=>
```

5080 BUFFER#####/AB
46638 LINK###/AB
L4 2 (LINK####/AB(3A)LIST/AB(3A)BUFFER#####/AB(P)LINK###/AB)

=> d cit ab 1-2

1. 5,682,553, Oct. 28, 1997, Host computer and network interface using a two-dimensional per-application list of application level free buffers; Randy B. Osborne, 395/876; 370/473; 395/200.64; 711/170, 171 [IMAGE AVAILABLE]

US PAT NO: 5,682,553 [IMAGE AVAILABLE] L4: 1 of 2

ABSTRACT:
A network interface using per-application free buffer lists includes a pat processor which processes an incoming message and stores packet data into free buffers designated for the application for which the message intended. The packet processor has memory storing an internal free buffer list. The internal free buffer list is loaded from an external free buffer list memory, which contains a free buffer list for each application. Each time a message arrives for a given application, the packet processor retrieves a portion of the external free buffer list for the application and loads the portion into the internal free buffer list. The portion which is loaded is a number of free buffers which is thought to be sufficient to handle an anticipated size of the incoming message. As a packet is processed, data are deposited in the buffers specified in the internal list. Any internal buffers unused after the packet is processed are attached to the end of the list of filled buffers returned, providing a self-cleaning property that allows an application to exert some control over which buffer an incoming packet uses. If packet data remains after the internal free buffer list is used up, the packet processor retrieves another portion of the external free buffer list and continues processing the message. To facilitate reading only a portion of the external free buffer list, the list may be organized as a two-dimensional structure, such as a **linked list** of free **buffer** lists.

2. 5,317,692, May 31, 1994, Method and apparatus for buffer chaining in a communications controller; James L. Ashton, et al., 711/5, 167 [IMAGE AVAILABLE]

US PAT NO: 5,317,692 [IMAGE AVAILABLE] L4: 2 of 2

ABSTRACT:
Method and apparatus in a communications controller to transfer data between a host computer and the controller. The communications controller includes a channel adapter (CA) and a central control unit (CCU) for controlling the operation of the CA. In response to a request from the CCU, the channel adapter transfers data between the host computer and the channel adapter to or from a **linked list** of **buffers** until all messages contained in the **linked** list have been transferred. Only after all messages in the present transmission have been transferred, the CA interrupts the CCU to signal completion. In a preferred embodiment, the channel adapter includes a microprocessor and a read-only-memory containing programmed instructions for controlling the microprocessor. Together, the microprocessor under control of the read-only-memory instructions form an apparatus for carrying out the method.

(FILE 'USPAT' ENTERED AT 16:30:03 ON 17 APR 1998)

L1 0 S LINK####(3A)LIST(3A)BUFFER#####(P)ISOCHRONOUS

L2 106 S LINK####(3A)LIST(3A)BUFFER#####(P)LINK###

L3 8 S LINK####(3A)LIST(3A)BUFFER#####(P)CONFIGUR#####

L6 27 S ISOCHRONOUS CHANNEL
L7 13 S L6 AND LINKED
L8 7 S L7 AND BUFFERS

=> d ab 1-

US PAT NO: 5,594,734 :IMAGE AVAILABLE: L8: 1 of 7

ABSTRACT:
A data communication system, such as a local area network, is provided with a capability of transmitting isochronous data. Preferably the system conveys both isochronous data and non-isochronous data by time-multiplexing the data into a recurring frame structure on a four-bit nibble basis. Switching of data is handled using switching tables. The tables can be updated by a processor. Updates can be performed asynchronously so that the processor does not have to wait until the switch tables are in an unused updatable state before outputting the update information. An efficient encoding scheme permits transmission of both isochronous and non-isochronous data over existing media, such as twisted pair, without degrading bandwidth previously achieved for non-isochronous data over the same media, such as using an Ethernet system. The arriving data is de-multiplexed at the hub into separate channels for handling the separate streams by appropriate hardware.

US PAT NO: 5,594,732 :IMAGE AVAILABLE: L8: 2 of 7

ABSTRACT:
A subsystem for communicating a private network signalling message over a packet network and bridges for communicating a Media Access Control (MAC) layer frame over an **isochronous channel** and for communicating an isochronous signalling frame over a nonisochronous network. The subsystem comprises: (1) an encapsulation circuit, coupled to a transmitting user station, capable of receiving the private network signalling message from the transmitting user station, the encapsulating circuit encapsulating the signalling message within, and adding source and destination addresses to, a routable protocol frame, the source and destination addresses corresponding to addresses of the transmitting user station and a particular receiving user station, the encapsulation circuit queuing the routable protocol frame for transmission over the packet network and (2) a de-encapsulation circuit, coupled to the particular receiving user station, capable of receiving the routable protocol frame, the de-encapsulation circuit extracting the signalling message from the routable protocol frame, the packet network thereby simulating a point-to-point connection between the transmitting and particular receiving user stations to effect node-to-node private network signalling